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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,073	12/01/2003	Eiji Ohta	09792909-5742	2729

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EXAMINER

WALSH, DANIEL I

ART UNIT	PAPER NUMBER
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2876

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No. 10/725,073	Applicant(s) OHTA ET AL.	
	Examiner Daniel I. Walsh	Art Unit 2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply.

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11-14-06 (RCE).
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,6-9 and 17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,6-9 and 17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Receipt is acknowledged of the RCE received on 11-14-06.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1, 7-9, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ota et al. (JP 2002-163624) in view of Kodai (US 5,026,452).

Ota et al teaches an IC card with an IC chip 5 mounted on an insulating substrate 1 having an antenna coil 3, and a chip reinforcing plate (9, 9') provided on at least an IC mounted surface of the insulating substrate 1, a core layer 13 comprising a plurality of sheet materials 15,16 having an IC module disposed there between. The plurality of sheet materials comprise a

pair of inner core sheets 15,16 that are adjacent to the IC module. Though Ota et al. is silent to through holes for the IC module, the examiner notes it is well known and conventional to have such a hole/recess in order to fit the IC module into the core, and therefore such modification is well known and conventional in the art, as an obvious expedient. For clarification purposes, the Examiner notes that FIG. 1 shows an arrangement where an IC chip and reinforcing plates are disposed in what appears to be a hole/cavity (interpreted as a through hole by the Examiner). In FIG. 1, the height of the hole on both sides appears to be substantially equal to that of the projections, thus satisfying the relationships set forth in the claims. The Examiner notes that as per FIG. 5 of the Applicants own Application, the projections are illustrated as being the distance between the insulating substrate and the reinforcing plate. Accordingly, the sum of the through holes (measured on both sides of the substrate), being substantially equal to the projection height, as the reinforcing plate is at the ends of the through holes, the limitations are met, as $B1+C1$ is seen as substantially equal to A , which places it in the claimed range. It is interpreted by the Examiner that upon formation of the card by pressure, that a through hole can be created. Additionally, the Examiner notes that the term "projection" is sufficiently broad. The claims have not recited what the projection is, and the Examiner notes that any reasonable interpretation can be applied by additional art, to meet the broad recitation of a projection.

Ota et al. is silent to the sheet materials have a hole formed before the chip is placed in.

Kodai et al. teaches such limitations (FIG. 7), where a through hole (7) is formed between layers of an IC card prior to chip insertion..

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Ota et al. with those of Kobayashi et al.

One would have been motivated to do this to accommodate the chip dimension to ensure smoothness of the IC card, as opposed to pressing/pressure as taught by Ota et al., that can lead to smoothness being compromised and possible deformation of the card or damaging the device.

Re claim 7, display layer 20 is a rewritable display layer.

Re claims 8-9, Ota et al. teaches the limitations (paragraph [0037]+)

Re claim 17, the limitations have been discussed above.

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ota et al./Ramachandran, as discussed above, in view of Saito et al. (JP 11078324).

The teachings of Ota et al./Ramachandran have been discussed above.

Ota et al./Ramachandran is silent to an outer core sheet stacked on at least one of the pair of inner core sheets.

Saito et al. teaches outer core sheets (SOLUTION).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Ota et al./Ramachandran with those of Saito et al.

One would have been motivated to do this to increase impact resistance strength and heat resistance/protection.

Response to Arguments

4. Applicant's arguments with respect to claims are moot in view of the new grounds of rejection (See above), where Kodai is applied to teach a through hole sized to the IC chip (before chip is placed in) so as to ensure smoothness of the card/reduce possible deformation/damage.

Additional Remarks

5. The Examiner notes that Usami et al., as cited previously, teaches that the size of an IC chip is in the range of 30 micrometers. Additionally, multilayered cards (sheets) are well known in the art (US 5,346,576 6,352,767, 5,888,624, 5,304,513, and 5,026,452) and Ramachandran teaches a hole in the layers before card insertion (cited by the Applicant JP 2003346112) as does Kobayashi et al.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure (See PTO-892).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel I. Walsh whose telephone number is (571) 272-2409. The examiner can normally be reached on M-F 7:30-4:00.

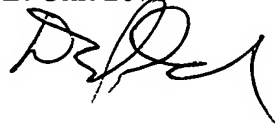
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel I Walsh

Examiner

Art Unit 2876



**DANIEL WALSH
PRIMARY EXAMINER**